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REMARKS

In an Office Action mailed April 2, 2003, claims 8-31 are pending wherein claims 1-7 were previously cancelled from a restriction requirement and claims 8-17 and 19-31 were rejected and claim 18 was objected to. In response, Applicants have amended claims 9, 11, 13, 17, 18, 21, 22, 24-29 and 31, cancelled claims 16 and 23 and are requesting reconsideration of the rejection and the allowance of the application.

The disclosure was objected to at pages 3 and 4 in the Brief Description of the Drawings section for using semicolons through the paragraph until the end of the last figure description rather than using periods. Conformance to this grammatical request is herein made to remove the objection.

Claims 9, 11, 18 and 23 were objected to for specifically enumerated informalities not related to the requirements for patentability. In claim 9, at line 5, an extraneous "and" is herein removed. A similar correction to claim 22 is also herein made. Claims 11 and 23 were objected for using the terminology "single-path components" and "multiple-path components" as used at page 10. FIG. 4 illustrates, for example, a multiple-path component logic block such as elements 63 and 64. Within each multiple-path component logic block are single-path component logic blocks such as single path component logic block 67. As stated at page 10, lines 12-14, single-path components and multiple-path components as described herein use conventional combinational logic elements. As stated at page 17, lines 13-15, "The present invention works for all types of designs...". The term "logic block" therefore clearly is defined to include any type of circuitry, whether performing a specific Boolean logic function or any other type of circuit

function. In order to conform claim terminology with the specification terminology that clearly defines 'logic block' as any type of circuitry, the claims are herein amended to recite "single-path component logic block" and "multiple-path component logic block". Additionally, in claim 18, the term "false path report" is incorporated into the claim. A report of the identified false paths is generated as indicated at page 8, lines 10-11. Correction to claim 13 by adding the limitation of generating a false path report is not required for clarity because the method of claim 13 recites a method for false path identification and concludes with the identification of a false path. Claim 18 recites generation of a false path report. With the amendments made herein, Applicants request the withdrawal of the stated objections.

Claims 21-31 are rejected under 35 U.S.C. 112, first paragraph, for reciting a design analysis tool stored on a computer readable medium. Claims 21, 22 and 24-31 are herein amended to remove reference to computer instructions and a computer readable medium. As amended, claims 21, 22 and 24-31 now clearly recite a method for identifying false paths that is fully enabled by Applicants' specification. Claim 24 recites a method for interfacing between a static analysis tool, the timing analysis 54 of FIG. 3, and an automatic test pattern generation (ATPG) tool, the ATPG 59 of FIG. 3. Applicants respectfully request the reconsideration and withdrawal of the 35 U.S.C. 112, first paragraph rejection.

Claims 11 and 23 were rejected under 35 U.S.C. 112, second paragraph, as being indefinite in connection with the terminology "logic blocks". The amendments referenced above regarding this terminology removes any potential for indefiniteness associated with this terminology as defined in the specification. Accordingly, Applicants request the removal of the rejection.

Claims 8-10, 12-17, 19 and 20 were rejected under 35 U.S.C. 102(a) as being anticipated by the Bhadra et al. paper. The author of the reference, Jayanta Bhadra, is a named Applicant herein and represents his work product as disclosed and recited in the rejected claims. Another author of the paper is Magdy S. Abadir, another named Applicant of this invention. Applicants respectfully submit this reference is not valid prior art for purposes of 35 U.S.C. 102(a) and therefore the rejection is improper and should be withdrawn.

In particular, Section 706.02(a), Section III. of the Manual of Patent Examining Procedure, provides a directive as to when 35 U.S.C. 102(a) may apply. Quoting therefrom, "For 35 U.S.C. 102(a) to apply, the reference must have a publication date earlier in time than the effective filing date of the application, and must not be applicant's own work." The Bhadra et al. paper relied upon in this rejection is Applicants' own work and was authored by Jayanta Bhadra and Magdy Abadir who are herein identified as inventors of the claimed subject matter. An additional author named in the Bhadra et al. paper, J.A. Abraham, did not invent the claimed subject matter of this application and therefore is not a listed Applicant. The common subject matter between the paper and all the pending claims is not attributable to J.A. Abraham. Accordingly, Applicants request the withdrawal of the 35 U.S.C. 102(a) rejection.

Additionally, the Bhadra et al. paper does not qualify as 35 U.S.C. 102(b) prior art as the Bhadra et al. paper was published less than one year before Applicants' filing date. The publication of the Bhadra et al. paper occurred on May 21, 2000 at the IEEE Custom Integrated Circuits Conference in Orlando, Florida. Evidence of this date is provided in Exhibit A attached hereto that is from the IEEE web site where a copy of Bhadra's paper may be obtained. Applicants' filing date is February 13, 2001, well within one year of the publication date.

Claim 18 was objected to as being allowable. In response, Applicants have represented claim 18 in independent form incorporating the base limitations and request the allowance thereof. Claim 11 was deemed allowable if amended to overcome the 35 U.S.C. 112, second paragraph, rejection. Therefore, Applicants request the allowance of claim 11.

All other claims herein are allowable over the prior art made of record. With the removal of Applicants' paper as a prior art reference, none of the art made of record recites a method for false path identification that interfaces between a static tool and an ATPG tool. For example, Applicants recite receiving a first set of paths corresponding to a circuit design, providing a set of conditions related to initial and final value, side propagation and slower path conditions corresponding to at least one path of the first set of paths to an automatic test pattern generation (ATPG) tool where the ATPG tool has an ATPG model corresponding to at least a portion of the circuit design. The prior art does not teach or suggest an ATPG tool that generates a response to this set of conditions using the ATPG model and identifies a false path within the first set of paths based on the response from the ATPG tool. Additionally, as noted in the Office Communication, no art made of record teaches or suggests feeding a false path report to a static analysis tool. The prior art also does not teach or suggest a method for interfacing between a static analysis tool and an ATPG tool as recited. Applicants therefore request the allowance of claims 8-15, 17-22 and 24-31.

No amendment made herein is related to the statutory requirements of patentability unless expressly stated herein. Further, no amendment herein is made for the purpose of narrowing the scope of any claim, unless Applicants have argued herein that such amendment was made to distinguish over a particular reference or combination of references. In view of the amendments and remarks

set forth herein, the application is believed to be in condition for allowance and a notice to that effect is solicited. Nonetheless, should any issues remain that might be subject to resolution through a telephonic interview, the Examiner is requested to telephone the undersigned at (512) 996-6839.

Respectfully submitted,

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A quick and inexpensive method to identify false critical paths using ATPG techniques: an experimen with a PowerPC™ microprocessor

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Abstract:
Static timing analysis tools are used by designers of high speed/high perform circuits to determine whether timing requirements are met. Timing analysis t can report critical paths which are characterized by a transition on each node the path, however, they cannot generate a "witness" vector which would sens that path. This gives rise to the possibility of having paths which are reported the static timing analysis tool as potential critical paths, whereas there exists vector sequence which can sensitize them. Our goal is to identify these "false critical timing paths" safely and without much overhead, so that the efforts n to redesign and/or optimize critical paths can be reduced. We have devised a simple technique using a tool that we have written and a commercial ATPG tc meet this goal. We applied the technique on the state of the art fourth gener MPC7400 PowerPC™ microprocessor designed at Motorola's PowerPC Design Center in Austin, TX. Our initial experimental results show the effectiveness o technique. The salient features of the technique are that it is both quick and inexpensive

Index Terms:
automatic test pattern generation integrated circuit testing logic testing microprocesso chips timing ATPG techniques MPC7400 Motorola PowerPC microprocessor fals critical paths identification

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